

REMARKS**Present Status of Application**

The Office Action mailed April 22, rejected claims 1 and 7 under 35 U.S.C. § 102(b), as being anticipated by Park (US Patent 6,100,559). Claims 2-6 and 8-13 were rejected under 35 U.S.C. § 103(a) over Park in view of Bui (US Patent 6,163,049). The Office Action objected drawings and the specification for informalities. Claims 1 and 7 have been amended, while claim 3 has been cancelled. This Amendment is promptly filed to place the above-captioned case in condition for allowance. No new matter has been added to the application by the amendments made to the claims, specification or otherwise in the application. After considering the following remarks, a notice of allowance is respectfully solicited.

Discussion of objections

The drawings were objected under 37 CFR 1.83(a) because the several reference signs were not present.

In response thereto, applicants have carefully reviewed the drawing figures, to eliminate the specific matter, and to ensure that there are no further similar errors present therein. Submitted for the Examiner's approval is the proposed drawing (Fig. 1) including proper labeling as suggested by the Office Action.

The specification was objected to because of informalities. In response thereto, proper correction has been made to the specification.

The Office Action objected the title of the invention as no being descriptive. Applicant respectfully disagrees and submits that since the claimed invention is directed to a flash memory structure, therefore Applicant respectfully submits that the original title of the invention is clearly indicative of the invention to which the claims are directed.

Reconsideration and withdrawal of these objections are respectfully requested.

Discussion for 35 USC 102 & 103 rejections

Claims 1 and 7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Park (US Patent 6,100,559).

The Office Action stated that Park disclose all the claimed features mentioned in claims 1 and 7.

Applicant respectfully traverses these rejections but has amended the independent claims 1 and 7 to more clearly define the method according to the present invention. As amended, claims 1 and 7 respectively recite:

1. A flash memory structure, comprising:
 - a tunneling oxide layer located upon a substrate;
 - a floating gate located upon the tunneling oxide layer;
 - a first oxide layer located upon the floating gate;
 - a high dielectric constant dielectric layer located upon the first oxide layer, *wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8*;
 - a second oxide layer, located upon the high dielectric constant dielectric layer, wherein, together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;
 - a control gate formed on the second oxide layer of the dielectric stacked layer; and
 - a source/drain region located in the substrate on the two sides of the floating gate.

7. A flash memory structure, comprising:
a tunneling oxide layer located upon a substrate;
a floating gate located upon the tunneling oxide layer;
a first oxide layer located upon the floating gate;
a high dielectric constant dielectric layer having a dielectric constant greater than 8 located upon the first oxide layer, wherein, together with the oxide layer, a dielectric stacked layer is formed;
a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and
a source/drain region located within the substrate on the two sides of the floating gate.
(Emphasis added)

Applicants submit that claims 1 and 7 patently define over the Park reference for at least the reason that the cited art fails to disclose at least the features emphasized above.

Park merely discloses a memory cell 8, including a doped substrate 12, a source/drain 13a, 13b, a tunnel oxide layer 15 and an interpoly dielectric 24 separating a floating gate 16 from a control gate 26. Floating gates are separated by field oxide layers 14a-b. It is noted that the interpoly dielectric 24 typically includes a plurality of films, such as, a bottom film of silicon dioxide, a middle film of silicon nitride and a top film of silicon dioxide. This type of interpoly dielectric is commonly referred to as an oxide-nitride-oxide (ONO) layer (Col. 2, lines 20-25). Moreover, even if the field oxides 14a-b were comparable, as considered by the Office Action, to the first oxide layer claimed in the invention, the high dielectric constant dielectric layer of the present invention is not equivalent to the ONO layer of Park's. Therefore, Park fails to teach or suggest a high dielectric constant dielectric layer having a dielectric constant larger than 8.

Reconsideration and withdrawal of this rejection is respectfully requested.

Claims 2-6 and 8-13 were rejected under 35 U.S.C. § 103(a) over Park in view of Bui (US

Patent 6,163,049).

The Office Action further relied on Bui for teaching the lacking features claimed in claims 2-6 and 8-13.

Applicant respectfully traverses these rejections for the following reasons. As amended, independent claims 1 and 7 further recites the feature “the high dielectric constant dielectric layer having a dielectric constant larger than 8”. As recognized by the Office Action, Park fails to teach “a band gap value of the high dielectric constant dielectric layer”, “the dielectric constant of the high dielectric constant dielectric layer” or “the material of the high dielectric constant dielectric layer”. The cited reference Bui is relied for teaching these features.

Bui teaches a composite ONO dielectric film 600 between a floating gate 500 and a control gate 700. The composite ONO film stack 600 includes a LPCVD silicon dioxide layer 601, a silicon nitride layer 602 and a second oxide layer 603 comprising a material with a dielectric constant greater than that of silicon dioxide, e.g., greater than about 10, such as aluminum oxide, titanium oxide or tantalum oxide. Alternatively, the composite ONO film stack 660 includes a first oxide layer 661, a silicon nitride layer 662 and a second oxide layer 663, while both oxide layers comprising a material with a dielectric constant greater than that of silicon dioxide, e.g., greater than about 10, such as aluminum oxide, titanium oxide or tantalum oxide. It is noted that Bui teaches the oxide/silicon nitride/oxide layer, with the **silicon nitride layer sandwiched between two oxide layers** as a composite film stack.

In fact, Bui teaches away from the present invention by suggesting the film stack consisting

of the silicon nitride layer sandwiched between two oxide layers, while the present invention discloses the dielectric stacked layer including at least the high dielectric constant dielectric layer and the oxide layer. The high dielectric constant dielectric layer of the present invention has a dielectric constant larger than 8. That is, the high dielectric constant dielectric layer is not possible to be a silicon nitride layer.

The Office Action considers it is obvious to modify the device of Park to include the aluminum oxide of Bui in order to maintain the capacitance of the ONO film. But that is hindsight rationalization not once mentioned in either Park or Bui, and contrary to the teachings of these references. Even if combined, Park and Bui do not achieve the claimed invention because Park merely discloses the silicon oxide/silicon nitride/silicon oxide (ONO) layer between the floating gate and the control gate and Bui suggests the silicon nitride layer sandwiched between two high dielectric oxide layers. Significantly, if you combine Park and Bui, a stacked ONO layer consisting of high dielectric constant oxide/silicon nitride/ high dielectric constant oxide is obtained. Therefore, the combination of Park and Bui would dissuade one of ordinary skill in the art from arriving at the present invention.

In determining whether even a *prima facie* showing of obviousness exists, it is necessary to ascertain whether the prior art teachings suggest the claimed combination to one of ordinary skill in the art. The burden of establishing a *prima facie* showing of obviousness rests upon the Patent Office, and that burden has not been met. The only suggestion to combine the various features from each patent comes from the applicant's specification and claims.

Applicant submits that claims 1, 7 and 13 patently defines over the cited references for at least the reason that the cited art fails to disclose at least the feature mentioned above. For at least the foregoing reasons, all pending claims patently define over the cited references and should be allowed. Accordingly, the rejection under § 103 should be withdrawn.

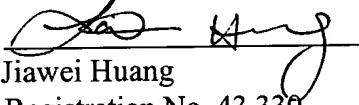
CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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VERSION WITH MARKINGS TO SHOW CHANGE**FOR THE SPECIFICATION:**

Please substitute the specification with the following paragraphs with the same numberings.

[0024] Moreover, whether or not to leave out the second oxide layer 216 between the high dielectric constant dielectric layer 214 and the control gate 208 within the dielectric stacked layer 210 is decided according to the band gap size of the high dielectric constant dielectric layer 214 used. If the band gap of the utilized high dielectric constant dielectric layer 214 is as wide or is wider than the silicon oxide band gap, then the second oxide layer 216 is left out. Alternately, if the band gap of the high dielectric constant dielectric layer 214 is less than [he]the silicon oxide band gap, then the second oxide layer 216 is included. Table 2 below indicates the band gap values of the utilized dielectric layer 214 material in the present embodiment and furthermore includes the band gap values of SiO_2 and Si_3N_4 .

[0026] As shown in Tables 1 and 2, the Al_2O_3 band gap is greater than the [Si_3N_4] $\text{Si}_3\text{N}_4/\text{SiO}_2$ band gap. Since the Al_2O_3 band gap is similar to the SiO_2 band gap, when using Al_2O_3 as the material of the dielectric layer 214, the other oxide layers 212 and 216 within the dielectric stacked layer 210 are replaced, thereby simplifying the manufacturing process of the flash memory.

FOR THE CLAIMS:

Claim 3 has been canceled without prejudice and disclaimer.

Claims 1 and 7 have been amended as follows:

1. (Once Amended) A flash memory structure, comprising:
a tunneling oxide layer located upon a substrate;
a floating gate located upon the tunneling oxide layer;

a first oxide layer located upon the floating gate;
a high dielectric constant dielectric layer located upon the first oxide layer, wherein a dielectric constant of the high dielectric constant dielectric layer is greater than 8;
a second oxide layer, located upon the high dielectric constant dielectric layer, wherein, together with the first oxide layer and the high dielectric constant dielectric layer, a dielectric stacked layer is formed;
a control gate formed on the second oxide layer of the dielectric stacked layer; and
a source/drain region located in the substrate on the two sides of the floating gate.

7. (Once Amended) A flash memory structure, comprising:
a tunneling oxide layer located upon a substrate;
a floating gate located upon the tunneling oxide layer;
a first oxide layer located upon the floating gate;
a high dielectric constant dielectric layer having a dielectric constant greater than 8 located upon the first oxide layer, wherein, together with the oxide layer, a dielectric stacked layer is formed;
a control gate formed on the high dielectric constant dielectric layer of the dielectric stacked layer; and
a source/drain region located within the substrate on the two sides of the floating gate.